IN THE CLAIMS:

Please amend claim 4 as shown in the complete list of claims that is presented below.

Claim 1 (cancelled).

2. (previously presented) The microcontroller of claim 4, wherein the control circuit further comprises a plurality of data latches for storing said part of the program.

3. (previously presented) The microcontroller of claim 4, wherein the control circuit further comprises a first-in-first-out memory for storing said part of the program.

4. (currently amended) A microcontroller comprising:

a central processing unit generating a first address signal and executing a program including an instruction that causes the central processing unit to activate a halt signal, to stop executing the program until an interrupt signal is received, and then to inactivate the halt signal;

a memory storing data including said program, receiving a mode signal, outputting the stored data when the mode signal is inactive, and discontinuing output of the stored data when the mode signal is active; and

a control circuit receiving the halt signal from the central processing unit, the control circuit including an address control unit generating a second address signal for reading ~~said~~ a part of the program, and a selector receiving the first address signal and the second address signal, selecting the first address signal when the halt signal is inactive, selecting the second address signal when the halt signal is active, and supplying the selected address signal to the memory,

wherein, when the halt signal is activated, the control circuit reads ~~a certain~~ said part of the program from the memory, internally stores said part of the program, then activates the mode signal, and

wherein, when the halt signal is inactivated, the control circuit inactivates the mode signal and supplies the central processing unit with the internally stored part of the program.

Claim 5 (cancelled).

6. (previously presented) The microcontroller of claim 10, wherein the control circuit further comprises a counter for generating a delay from input of the interrupt signal to output of the interrupt signal.

7. (previously presented) The microcontroller of claim 6, wherein the control circuit further comprises a logic gate for passing the interrupt signal to the central processing unit, said logic gate receiving the interrupt signal and an output signal from the counter.

Claim 8 (cancelled).

9. (previously presented) A microcontroller comprising:

a central processing unit executing a program including an instruction that causes the central processing unit to activate a halt signal, to stop executing the program until an interrupt signal is received, and then to inactivate the halt signal;

a memory storing data including said program, receiving a mode signal, outputting the stored data when the mode signal is inactive, discontinuing output of the stored data when the mode signal is active, and generating a busy signal indicating whether the memory is ready to resume data output; and

a control circuit receiving the busy signal and the interrupt signal, the control circuit including a flip-flop delaying said busy signal, an inverter inverting said busy signal, and a logic gate for passing the interrupt signal to the central processing unit, said logic gate receiving the interrupt signal, the delayed busy signal from the flip-flop, and the inverted busy signal from the inverter,

wherein, when the halt signal is activated, the control circuit activates the mode signal, and

wherein, when the control circuit receives the interrupt signal, the control circuit inactivates the mode signal, waits for the memory to resume data output, and then sends the interrupt signal to the central processing unit.

10. (previously presented) A microcontroller comprising:

a central processing unit executing a program including an instruction that causes the central processing unit to activate a halt signal, to stop executing the program until an interrupt signal is received, and then to inactivate the halt signal;

a memory storing data including said program, receiving a mode signal, outputting the stored data when the mode signal is inactive, and discontinuing output of the stored data when the mode signal is active; and

a control circuit through which the interrupt signal is passed to the central processing unit, the control circuit including a flip-flop for generating the mode signal, said flip-flop being set by the halt signal and reset by the interrupt signal,

wherein, when the halt signal is activated, the control circuit activates the mode signal, and

wherein, when the control circuit receives the interrupt signal, the control circuit inactivates the mode signal, waits for the memory to resume data output, and then sends the interrupt signal to the central processing unit.